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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,193	01/20/2004	Tsutomu Yamada	500.43408X00	7703

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EXAMINER	
BORKOWSKI, ROBERT	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,193	YAMADA ET AL.	
	Examiner	Art Unit	
	Robert Borkowski	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-2, 4-12, 14-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Kiremidjian (U.S. Patent No. 4,727,475).

Regarding claims 1, 4, 14 Kiremidjian discloses a modular computer system (column 4 lines 25-38, Fig, 1) formed by connecting a processing module (column 4 lines 25-38, Fig. 1 element 15) having a processor mounted thereon and a plurality of I/O modules (column 4 lines 25-44, Fig. 1 elemens16-18) in a stacked form via connectors forming a bus (column 4 line 45 thru column 5 line 4, Fig. 1 element 11), wherein each of said I/O modules comprises:

a module exclusive selection part (column 1 lines 47-59) for activating a module select signal input from a terminal in a position on a processing module side connector (column 5 lines 39-52), the position being the same for said I/O modules (column 5 lines 53-66 "XPOUT signal serves as the XPIN signal to the downstream module"); and

an ID output part for outputting identification information (Fig. 4 element 21) of its own I/O module (column 5 lines 5-18) to a predetermined terminal on the connector

(column 5 lines 5-18, Fig. 4 element 20) on the basis of a module select activate signal output from said module exclusive selection part (column 5 lines 39-66).

Regarding claim 2, Kiremidjian discloses wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected (column 6 lines 37-55, Fig. 4); and

an ID input part for taking in the identification information (column 6 lines 37-55) output to the predetermined terminal on the connector (Fig, 4 element 20), and

said module select signal output part outputs the module select signal successively to the I/O modules connected to the processing modules (column 5 lines 39-66, column 7 lines 15-26, Fig. 4), and

said ID input part recognized the I/O modules and the identification information in association in accordance with an output order of the module select signal (column 5 lines 39-66).

Regarding claim 5, 15, Kiremidjian discloses wherein

said module exclusive selection part has a plurality of wires connected to a plurality of connector terminals on the processing module side (column 6 lines 37-55, Fig. 4),

one of the wires is connected to said ID output part (Fig. 4 element XIORD), and

one of other wires is connected to a terminal that is included in a plurality of connector terminals on a side opposite to the processing module and that is in the same

position as that of the connector terminal supplies with a module select signal that selects its own module (column 5 lines 39-66, Fig. 4).

Regarding claim 6, 16, Kiremidjian discloses wherein said module exclusive selection part is formed by connecting a D terminal of a D type flip-flop to one of connector terminals on the processing module side (column 5 lines 39-66, Fig. 4 signal "XPIN+"), connecting a Q output terminal of said D type flip-flop to said ID output part (column 5 lines 39-66, Fig. 4 "a Q- output coupled as one input to NAND gate 32 ") and to a terminal that is included in connector terminals on a side opposite to the processing module and that is in the same position as that of connector terminal to which the D terminal is connected, and connecting a clock terminal of said D type flip-flop to a terminal to which connector terminals on the processing module side and the side opposite to the processing module are connected in common (column 5 lines 19-66, Fig. 4 element XIOWR "control signal supplied to the polling logic in each module").

Regarding claim 7, 17, Kiremidjian discloses wherein said processing module drives the connector terminal to which the clock terminal is connector terminal to which the D terminal is connected, with an enable signal (column 6 line 37 thru column 7 line 14, Fig. 4 element XIOWR "control signal supplied to the polling logic in each module").

Regarding claim 8, 18, Kiremidjian discloses wherein said ID output part comprises:

an ID generation part (Fig. 4 element 21) for generating identification information of its own module (column 5 lines 5-18); and

an output enable part (column 6 lines 37-55, Fig. 4 element 32 "ID ENABLE") for outputting the identification information generated by said ID generation part to a predetermined terminal on the connector (column 5 lines 5-18, Fig. 4 element 20).

Regarding claim 9, 19, Kiremidjian discloses wherein said ID output part comprises gate elements that are supplied with the identification information as inputs thereof and that are enabled by the active signal (column 5 lines 5-18).

Regarding claim 10, Kiremidjian discloses wherein said ID generation part generates the identification information as a serial signal on the basis of the activate signal and a clock signal (column 2 lines 51-59 "serial interconnection").

Regarding claim 11, 20, Kiremidjian discloses wherein said ID output part is formed by connecting wires driven by the activate signal to a plurality of predetermined terminals on the connector via PN-junction elements according to the identification information (column 5 lines 5-18).

Regarding claim 12, Kiremidjian discloses wherein said processing module comprises:

a module select signal output part for outputting the module select signal to a connector terminal to which the I/O module is connected (column 6 lines 37-55, Fig. 4); and

an ID input part for taking in the identification information (column 6 lines 37-55) output to the predetermined terminal on the connector (Fig, 4 element 20), and

said module select signal output part outputs the module select signal successively (column 7 lines 15-26) to the I/O modules connected to the processing module, and

said ID input part recognizes the I/O modules and the identification information in association in accordance with an output order of the module select signal (column 7 lines 15-26).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiremidjian (U.S. Patent No. 4,727,475) in view of Richman et al. (U.S. Patent No. 6,003,097).

Regarding claims 3, 13, Kiremidjian teaches a modular computer system (column 4 lines 25-38, Fig, 1) formed by connecting a processing module (column 4 lines 25-38, Fig. 1 element 15) and a plurality of I/O modules (column 4 lines 25-44, Fig. 1 elemens16-18). However, Kiremidjian is silent wherein in accordance with the association of the I/O modules with the identification information, said processing module reads preset bus configuration parameters and device drivers of the I/O modules from a memory, and accesses the I/O modules.

Richman et al. discloses wherein in accordance with the association of the I/O modules (see Richman et al. column 16 lines 15-34) with the identification information (see Richman et al. column 4 lines 11-26), said processing module reads preset bus configuration parameters and device drivers of the I/O modules from a memory (see Richman et al. column 4 line 66 thru column 5line 9), and accesses the I/O modules (see Richman et al. column 15 lines 25-46).

One of ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Kiremidjian use the association of the I/O modules with the identification information to configure parameters and device drivers of the I/O modules from a memory in order to enable the system to determine and establish a working configuration for all devices connected to the computer, and to load the appropriate device drivers without substantial user intervention (see Richman et al. column 3 lines 13-27).

It is for this reason that one of ordinary skill in the art be motivated to implement Kiremidjian method with the association of the I/O modules with the identification information to configure parameters and device drivers of the I/O modules from a memory in order to enable the system to determine and establish a working configuration for all devices connected to the computer, and to load the appropriate device drivers without substantial user intervention (see Richman et al. column 3 lines 13-27).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made of record of to further show the system for allocating resources in a modular computer.

1) Martinez et al. U.S. Patent No. 5,790,782

2) Patel U.S. Patent No. 5,999,989

3) Katz et al. U.S. Patent App. Pub. No. 2002/0065950

4) Wilson et al. U.S. Patent App. Pub. No. 2003/0041088

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Borkowski whose telephone number is 571-272-8626. The examiner can normally be reached on Monday - Friday 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM NGOC (KIM) HUYNH can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KIM HUYNH
SUPERVISORY PATENT EXAMINER
3/3/06

Robert Borkowski
Art Unit 2181
March 1, 2006